UTILITY PATENT APPLICATION TRANSMITTAL

(Only for new nonprovisional applications under 37 CFR 1.53(b))

Attorney Docket No.	A0312/7363/RJP
First Named Inventor or Application Identifier	
NAKAMURA, Katsufumi	
Express Mail Label No.	EM192719915US
Date of Deposit	May 26, 2000

APPLICATION ELEMENTS

See MPEP chapter 600 concerning utility patent application contents

1. ☐ Fee Transmittal Form
   (Submit an original, and a duplicate for fee processing)
2. ☒ Specification [Total pages 10]
   7 - pages specification
   1 - pages abstract
   2 - pages claims 12 - Total claims
3. ☒ Drawing(s) *(35 USC 113)* [Total sheets 12]
   ☒ Informal ☐ Formal [Total drawings 11]
4. ☐ Oath or Declaration [Total pages 0]
   a. ☐ Newly executed (original or copy)
   b. ☐ Unsigned
   c. ☐ Copy from a prior application (37 CFR 1.63(d))
   (for continuation/divisional with Box 17 completed)
   [Note Box 5 below]
   i. ☐ DELETION OF INVENTOR(S)
   Signed statement attached deleting inventor(s) named in the prior application, see 37 CFR 1.63(d)(2) and 1.33(b).
5. ☐ Incorporation by Reference
   (usable if Box 4b is checked)
   The entire disclosure of the prior application, from which a copy of the oath or declaration is supplied under Box 4b, is considered as being part of the disclosure of the accompanying application and is hereby incorporated by reference therein.

ADDRESS TO: **Box Patent Application**
Assistant Commissioner for Patents
Washington, DC 20231

6. ☐ Microfiche Computer Program (Appendix)
7. ☐ Nucleotide and/or Amino Acid Sequence Submission (if applicable, all necessary)
   a. ☐ Computer Readable Copy
   b. ☐ Paper Copy (identical to computer copy)
   c. ☐ Statement verifying identity of above copies

ACCOMPANYING APPLICATION PARTS

8. ☐ Assignment Papers/cover sheet & documents(s)
9. ☐ 37 CFR 3.73(b) Statement
   (when there is an assignee)
   ☐ Power of Attorney
10. ☐ English Translation of Document *(if applicable)*
11. ☐ Information Disclosure Statement PTO-1449
    ☐ Copies of IDS Citations
12. ☐ Preliminary Amendment
13. ☒ Return Receipt Postcard (MPEP 503)
    (Should be specifically itemized)
14. ☐ Small Entity Statement(s)
    ☐ Statement filed in prior application, Status still proper and desired
15. ☐ Certified Copy of Priority Document(s)
    (if foreign priority is claimed)

16. Other:

458628.1

17. If a CONTINUING APPLICATION, check appropriate box and supply the requisite information:

☐ Continuation ☐ Divisional ☐ Continuation-in-part (CIP) of prior application No.:

☐ Cancel in this application original claims of the prior application before calculating the filing fee.

☐ Amend the specification by inserting before the first line the sentence:

This application is a ☐ continuation ☐ divisional of application serial no. , filed , entitled , and now .

18. CORRESPONDENCE ADDRESS					
Correspondence address below					
ATTORNEY'S NAME	Randy J. Pritzker, Reg. No. 35,986				
NAME	Wolf, Greenfield & Sacks, P.C.				
ADDRESS	600 Atlantic Avenue				
CITY	Boston	***STATE***	MA	***ZIP***	02210
COUNTRY	USA	***TELEPHONE***	(617) 720-3500	***FAX***	(617) 720-2441

19. SIGNATURE OF APPLICANT, ATTORNEY, OR AGENT REQUIRED	
NAME	Randy J. Pritzker, Reg. No. 35,986
SIGNATURE	Randy J. Pritzker
DATE	May 26, 2000

PIXEL GAIN AMPLIFIER

Related Application

This application claims the benefit, under 35 U.S.C. §119(e), of the filing date of provisional application serial number 60/138,960, filed June 11, 1999.

Field of the Invention

The present invention is related to a programmable gain amplifier.

Background

A charge-coupled device (CCD) output waveform is a sequence of pixels, where each pixel is represented as the difference between a reset level and a data level. This signal waveform is initially processed before being passed on to the automatic gain control (AGC) circuit:

The data level is subtracted from the reset level on a pixel-by-pixel basis to remove the reset noise component common to both signals. This operation is called correlated double-sampling (CDS).

One prior art CDS is shown in block diagram form in Fig. 1. This is a pipelined CDS circuit. It has two non-overlapping time phases of operation: In the Q1 phase of the pipelined CDS circuit, the reset level is sampled by sample-and-hold (S/H) #1. A schematic diagram of a typical S/H is shown in Fig. 2. In the Q2 phase, the data level is sampled by S/H #2. Simultaneously, S/H #3 samples the output of S/H #1.

Drawbacks of the pipelined CDS technique are: (1) there are three sampling operations, which increases the noise over techniques requiring only two sampling operations; and (2) any gain or offset mismatch between the reset path (S/H #1 and S/H #3) and the data path (S/H #2) limits the ability of the CDS to remove reset noise.

Another prior art CDS is shown in Fig. 3. This is a dual CDS circuit.

S/H #1 and S/H #2 form a single CDS circuit, and S/H #3 and S/H #4 form a second single CDS circuit. Each single CDS processes alternate pixels. Thus, two CDS circuits are required to process all pixels.

The dual CDS has four phases of operation. In the Q1A phase, the reset level of the first pixel is sampled by S/H #1. The output switch is set to B. In the Q1B phase, the data level

of the first pixel is sampled by S/H #2. The output switch is set to B. In the Q2A phase, the reset level of the second pixel is sampled by S/H #3. The output switch is set to A. In the Q2B phase, the data level of the second pixel is sampled by S/H #4. The output switch is set to A.

Compared to the pipeline CDS of Fig. 1, the dual CDS has lower noise because only two sampling operations are performed for each pixel. Also, the AGC has a full period to sample each pixel.

Drawbacks of the dual CDS scheme include: (1) two CDS circuits are required because the previous pixel value must be held while the reset level of the next pixel is sampled; and (2) even and odd pixels use different CDS circuits, causing gain and offset errors which must be removed.

Summary

Applicants herein have discovered that in both prior art techniques, it is difficult to apply a variable pixel gain within the CDS.

The present invention is directed to a programmable gain amplifier. In one embodiment, a gain of the amplifier is programmable on a sample-by-sample basis.

The pixel-gain amplifier (PxGA), according to the present invention, may be used to apply a gain, which may be programmed on a pixel-by-pixel basis. This enables a user to compensate for differences in the average signal level between pixels of different colors.

One embodiment of the invention is directed to a pixel gain amplifier circuit including an amplifier having an input and an output. An input capacitor, coupled to the input of the amplifier, samples an input pixel during a first of first and second time phases. A feedback capacitor, coupled between the input and the output of the amplifier, receives charge from the input capacitor during the second time phase.

Another embodiment of the invention is directed to a method of sampling input pixels comprising the steps of: sampling an input pixel during a first of first and second time phases; amplifying the sampled input pixel during the second time phase; and controlling a gain of the amplification for each pixel.

A further embodiment of the invention is a means for varying a gain of an amplifier in a circuit according to a rapid rate. The means may include using a capacitor array. The means may include corresponding the rapid rate to the rate at which pixels are input into the circuit.

Brief Description of the Drawings

For a better understanding of the present invention, reference is made to the accompanying drawings, which are incorporated herein by reference and in which:

Fig. 1 is a block diagram of a pipeline CDS circuit according to the prior art;

Fig. 2 is a block diagram of a sample and hold circuit according to the prior art;

Fig. 3 is a block diagram of a dual CDS circuit according to the prior art;

Fig. 4 is a diagram of pixels processed in a CCD signal processing channel according to the prior art;

Fig. 5 is a diagram of pixels processed by a pixel gain amplifier;

Fig. 6 is a diagram of pixels processed in a CCD signal processing channel using a pixel gain amplifier;

Fig. 7 is a multiplexed gain amplifier according to the prior art;

Fig. 8(a) is a block diagram of a pixel gain amplifier circuit;

Fig. 8(b) is a block diagram of a pixel gain amplifier circuit in the first phase;

Fig. 8(c) is a block diagram of a pixel gain amplifier circuit in the second phase;

Fig. 9 is a block diagram of a CDS / PxGA circuit;

Fig. 10 is a block diagram of a CDS / PxGA circuit with offset correction;

Fig. 11 is a block diagram of a CDS / PxGA amplifier circuit with an expanded diagram of the feedback capacitor array.

Detailed Description

In addition to the drawbacks of the prior art CDS circuits mentioned above, schemes that correct for errors in a CCD signal neglect the varying amplitudes of the individual pixels which comprise the signal. CCDs utilize color filters to obtain color information. The CCD has different sensitivities to different colors, and as a result, the output amplitude of each pixel will depend not only on the amount of light to which it was exposed, but also on its particular color filter. For example, green pixels typically have a greater amplitude than blue

or red pixels. An example of this is shown in Fig. 4. At the output of the CDS 400 four example pixels 410 are shown. Each of these pixels has a different amplitude corresponding to their color: G represents a green pixel, R represents a red pixel, Ye represents a yellow pixel, and B represents a blue pixel. In signal processing of the prior art the pixels 410 are input into a variable gain amplifier 402 to yield amplified pixels 420. As a result of being amplified, each pixel gains a certain amount of noise 422. That noise 422 has the same magnitude for each pixel and is carried through the signal processing channel. Because the pixels have the same amount of noise but different amplitudes, each pixel has a different signal-to-noise ratio. Because the gain of the VGA 402 is limited by the amplitude of the brightest pixel, the pixels which are not as bright are not amplified as much as they could be to achieve the best signal-to-noise ratio.

After the signals are converted by the ADC 404, they still carry with them the noise 422 that was added by the VGA 402. A digital signal processor 406 is typically used to scale the varying amplitudes of the pixels 420 to an equivalent level 430, but the DSP 406 is unable to reduce the noise that the pixels gained in the analog domain. Because the scaling is done to bring each pixel to the same amplitude, the pixels with lower amplitude have a much greater resultant noise 432 than those pixels which started with a greater amplitude.

The only way to avoid the uneven signal-to-noise ratios is to scale the varying amplitudes of the pixels before they are amplified by the VGA 402. This will give each pixel the maximum amount of amplification without saturating the ADC. In order to do this, it must be possible to vary the gain of the amplifier from pixel-to-pixel.

A pixel gain amplifier (PxGA) is offered for this purpose. As shown in Fig. 5, the pixel gain amplifier 500 takes pixels of varying amplitude in input pixel data 510, amplifies each of them by the separate programmable gain 520 to yield the output pixel data 530 wherein each pixel has the same amplitude. For example, for pixel n 512 a gain of g0 522 is applied to yield the final pixel n*g0 532; for pixel n+1 514 gain g1 524 is applied to yield pixel (n+1)*g1 534, and so forth for the remaining pixels.

Fig. 6 shows a CCD signal processing channel with the PxGA. The input signal of pixels with varying amplitude 410 is input into the CDS 400. The output of the CDS is sent to the PxGA 500 where the pixels are amplified and scaled to an equal level. The pixel signals 604, along with a slight level of noise 602, are sent to the variable gain amplifier 402

where they are further amplified into the amplified signal 608 plus noise 606. By inserting the PxGA 500 into the channel, the signal-to-noise ratio has been increased for the color pixels which have inherently less sensitivity, yielding a constant signal-to-noise ratio for each pixel. The constant signal-to-noise ratio across pixels allows the ADC 404 to fully utilize its dynamic range.

In order to implement the channel of Fig. 6, the pixel gain amplifier must be able to alter its gain with sufficient speed so that each pixel is appropriately amplified. Prior art amplifiers are insufficient for this purpose.

Fig. 7 shows a multiplexed gain amplifier from the prior art. This example of an insufficient amplifier is a large circuit requiring multiple channels which consumes a great deal of power. Furthermore, each individual gain amplifier 701, 702, 703, etc., creates its own individual offset; each gain amplifier offset is different than the next, which leads to a mismatch of offsets to the output of a multiplexed gain amplifier. The non-linearity of the amplifier of Fig. 7 serves to further decrease its performance and make it unsuitable for the high speed variable gain task required by a CCD input.

The PxGA offered is suitable for high speed variable gain tasks such as image applications (e.g., image sensors) for pixel sampling, wherein the gain of the PxGA is programmable on a pixel-by-pixel basis. It should be appreciated that the invention is not so limited to this particular embodiment. For example, the invention need not be limited to image applications in which pixels are sampled.

One embodiment described herein is directed to a switched-capacitor amplifier circuit for sampling input voltages. Again, the invention need not be limited to a switched-capacitor circuit.

Figure 8 shows simplified diagrams for a switched-capacitor circuit, according to one embodiment, which performs pixel gain. This circuit employs two time phases (q1 and q2) of operation.

In the reset (q1) phase, shown in Fig. 8(b), the main amplifier 800 is placed in unity-gain feedback to provide a virtual ground at the summing node. The sampling capacitor 802 samples the input 806 and the feedback capacitor 804 samples a reference voltage 808.

In the data (q2) phase, shown in Fig. 8(c), the feedback capacitor 804 is placed in feedback around the main amp 800 and the voltage applied to the sampling capacitor 802

changes by input-reference1. Reference1 810 is a DC bias reference voltage. This forces a charge $\Delta Q = Cs$ (input-reference1) to shift from Cs 802 to Cfb 804, resulting in an output signal of (Cs / Cfb)(input-reference1).

By changing the capacitance values on the sampling capacitor 802 and/or the feedback capacitor 804, Cs and/or Cfb from pixel-to-pixel, the gain can be changed at the pixel rate. The input sampling capacitor 802 and/or the feedback capacitor 804 may be variable for this purpose. The gain control input 812 provides gain information which, in combination with the instantaneous digital switching, controls the capacitor gain.

With a restructuring of the circuit of Fig. 8, a circuit which performs the function of both a PxGA and a CDS is created. The circuit of Fig. 9 shows the combination. Since the architecture of Fig. 9 can simultaneously implement the CDS and PxGA functions, it will be referred to as a CDS/PxGA.

Figure 10 shows a scheme for implementing offset correction in this CDS/PxGA. Offset correction prevents the AGC from saturating when large gains are applied to small-amplitude input signals. The offset correction circuit 1000 samples the CDS/PxGA output and applies a correction signal to the summing node. The magnitude and sign of the correction signal is the same for all pixels, and is chosen so that during a "dummy clamp" interval where the input signal corresponds to black pixels, the output is zero. The preferred implementation of this offset correction circuit 1000 is with a fixed-value sampling capacitor Cs 1002, as indicated in Fig. 10.

Figure 11 shows one implementation for the variable feedback capacitor. There is a separate capacitor Cfb,i in the cap array for each gain setting i, $0 < i < n$, and the capacitors are used cumulatively: the i-th gain setting places Cfb,0, Cfb,1, ... Cfb,i in feedback, and the total feedback capacitance Cfb is the sum of these capacitors. The bits ci determine the gain setting. Note that Cfb,0 is always placed in feedback in the q2 phase, so there is always at least one capacitor in the feedback capacitor array.

Advantages of the CDS/PxGA include: (a) the PxGA operation is performed simultaneously with the CDS operation, so no extra circuit is required; (b) a simple method can be used for offset correction, independent of pixel gain; (c) the PxGA gain curve is guaranteed monotonic; and (d) all pixels are processed through the same signal path, avoiding pixel-to-pixel offset.

Having thus described at least one illustrative embodiment of the invention, various alterations, modifications and improvements will readily occur to those skilled in the art. Such alterations, modifications and improvements are intended to be within the spirit and scope of the invention. For example, the invention need not be limited to image applications in which pixels are sampled, nor need it be limited to a switched capacitor circuit. Accordingly, the foregoing description is by way of example only and is not intended as limiting. The invention is limited only as defined in the following claims and the equivalents thereto.

What is claimed is:

CLAIMS

1. A pixel gain amplifier circuit comprising:

an amplifier having an input and an output;

an input capacitor, coupled to the input of the amplifier, onto which input capacitor charge from an input pixel is sampled during a first of first and second time phases; and

a feedback capacitor, coupled between the input and the output of the amplifier, that receives charge from the input capacitor during the second time phase.

2. The pixel gain amplifier circuit as claimed in claim 1 wherein the input capacitor includes a variable capacitor.

3. The pixel gain amplifier circuit as claimed in claim 2 wherein the input capacitor comprises a capacitor array.

4. The pixel gain amplifier circuit of claims 2 or 3 wherein a capacitance of the input capacitor changes at a rate corresponding to a rate at which pixels are input into the circuit.

5. The pixel gain amplifier circuit as claimed in claim 1 wherein the feedback capacitor includes a variable capacitor.

6. The pixel gain amplifier circuit as claimed in claim 5 wherein the feedback capacitor comprises a capacitor array.

7. The pixel gain amplifier circuit of claims 5 or 6 wherein a capacitance of the feedback capacitor changes at a rate corresponding to a rate at which pixels are input into the circuit.

8. The pixel gain amplifier circuit as claimed in claim 1 further comprising an offset correction circuit.

9. A method of amplifying input pixels comprising the steps of:
sampling an input pixel during a first of first and second time phases;
amplifying the sampled input pixel during the second time phase; and
controlling a gain of the amplification for each pixel.

10. A pixel gain amplifier circuit comprising:
an amplifier having an input, an output and a gain;
means for varying the gain of the amplifier according to a rigid rate.

11. The pixel gain amplifier circuit according to claim 10 wherein the means for varying the gain of the amplifier includes a capacitor array.

12. The pixel gain amplifier circuit according to claim 10 wherein the rapid rate corresponds to a rate at which pixels are input into the circuit.

ABSTRACT

A correlated double sampling pixel gain amplifier includes a main amplifier, an input sampling capacitor, and a feedback capacitor. The input capacitor samples the inputs signal during a first time phase and the feedback capacitor samples the input during a second time phase. No sampling switch is located between the input capacitor and the input terminal. The feedback capacitor may include a capacitor array.

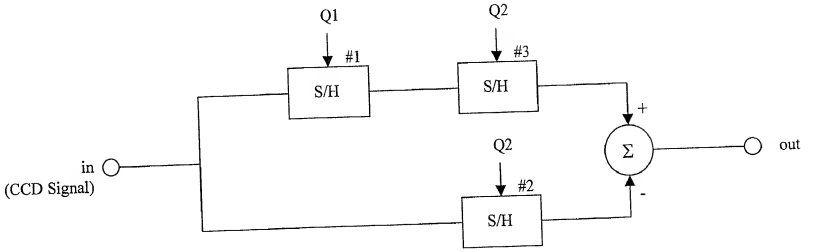


Figure 1: Pipeline CDS Circuit (Prior Art)

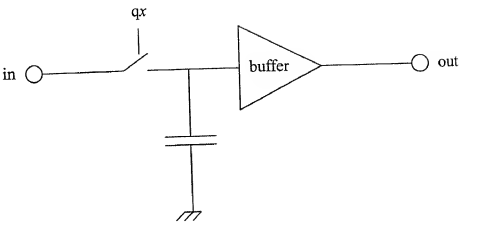


Figure 2: Sample-and-Hold (S/H) Circuit (Prior Art)

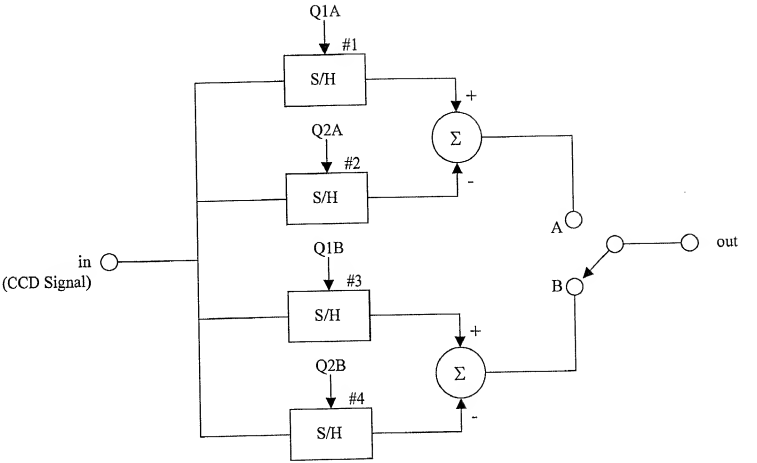


Figure 3: Dual CDS Circuit (Prior Art)

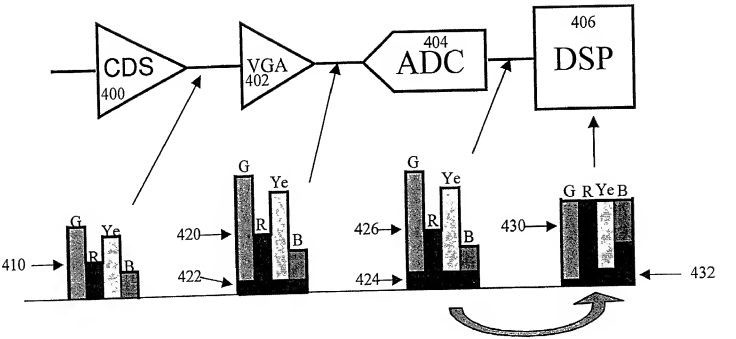


Figure 4: CCD Signal Processing Channel (Prior Art)

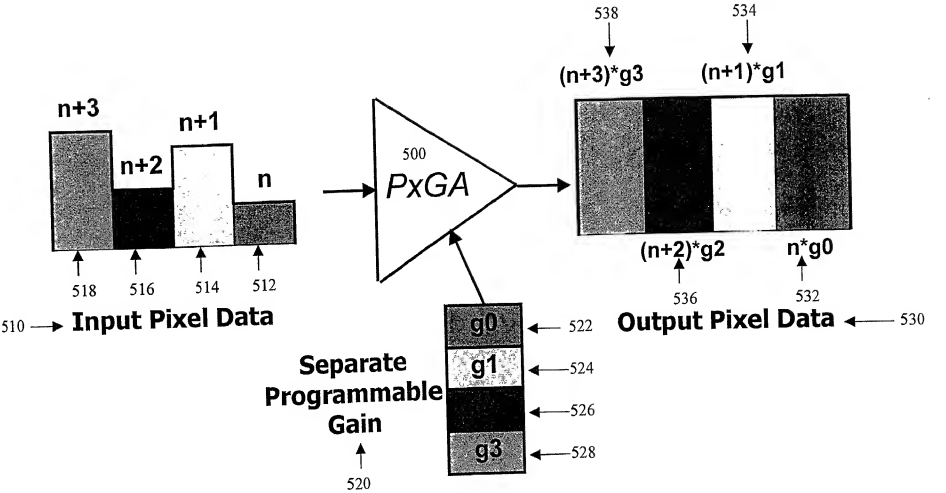


Figure 5: Pixel Gain Amplifier (PxGA)

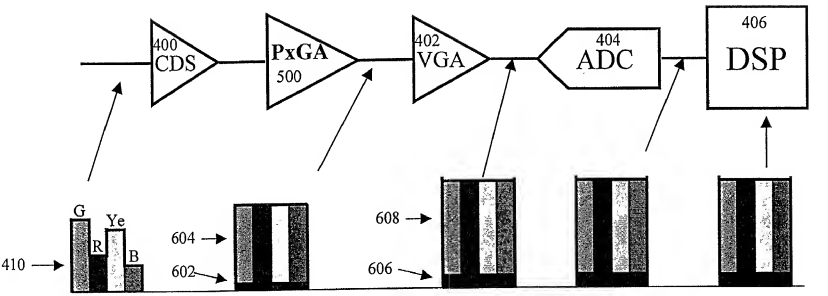


Figure 6: CCD Signal Processing Channel with PxGA

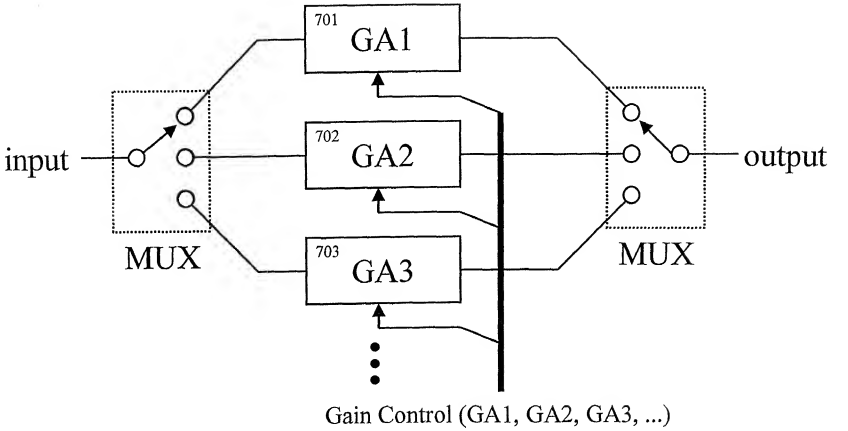


Figure 7: Multiplexed Gain Amplifier (Prior Art)

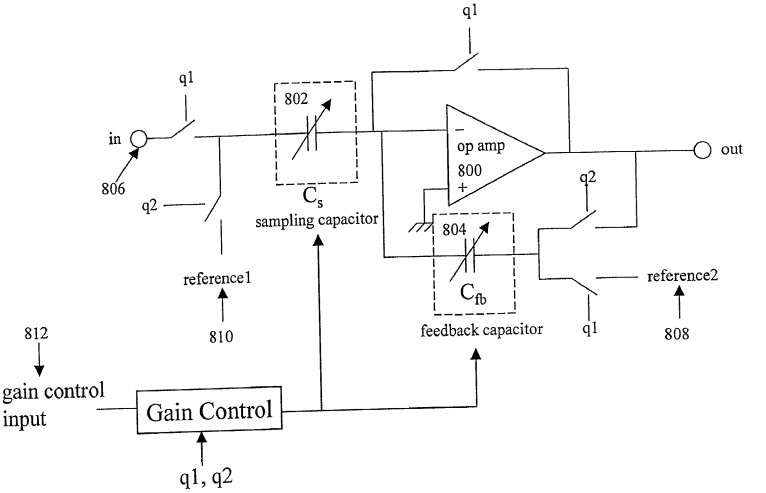


Figure 8(a): PxGA schematic

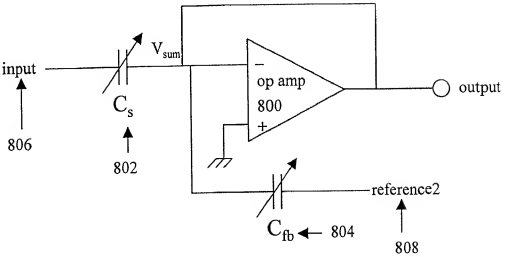


Figure 8(b): PxGA in q1 phase

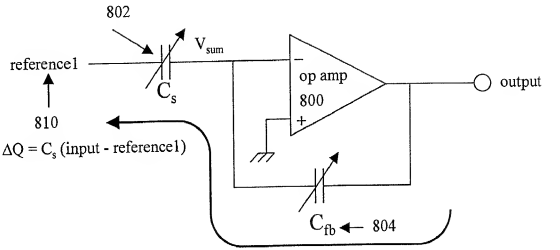


Figure 8(c): PxGA in q2 phase

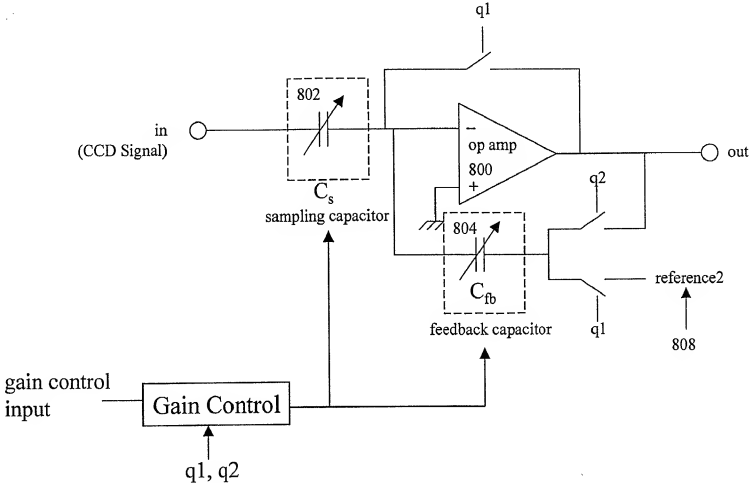


Figure 9: CDS/PxGA schematic

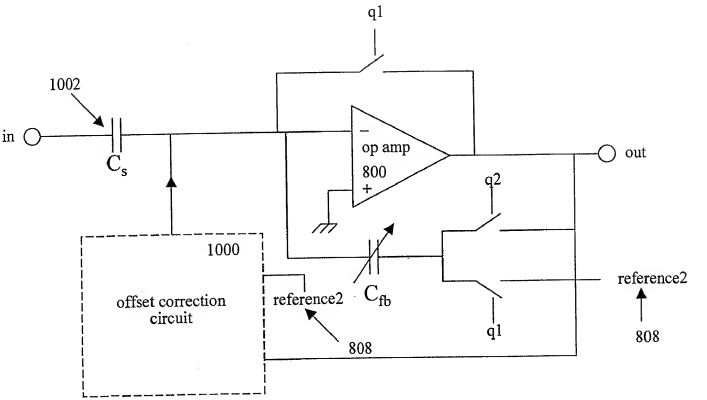


Figure 10: CDS/PxGA Circuit With Offset Correction

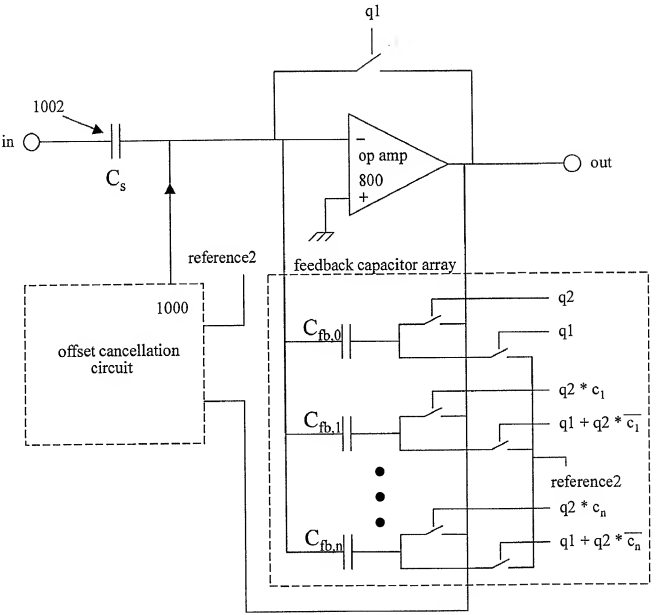
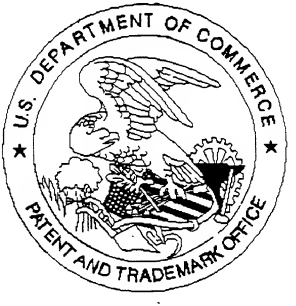


Figure 11: Implementation of Feedback Capacitor Array

United States Patent & Trademark Office

Office of Initial Patent Examination -- Scanning Division



Application deficiencies were found during scanning:

☑ Page(s) 3 of Transmittal were not present for scanning.
(Document title)

☐ Page(s)_____ of _____ were not present for scanning.
(Document title)

☐ Scanned copy is best available.